**Laboratory Experiment 4**

**EE348L**

**B. Madhavan**

**Revised by: Aaron Curry**

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**4 Experiment #4: Diodes**

**4.1 Introduction**

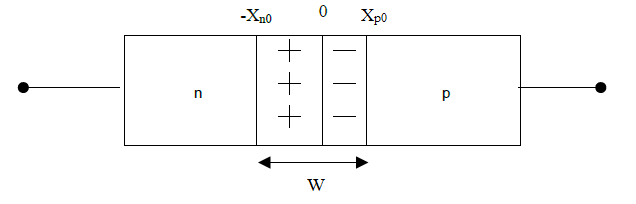
Diodes are among the most common electronic devices used in circuit design. Qualitatively, basic diode operation is best understood by a valve analogy. An ideal valve permits uninhibited fluid flow in one direction (provided the fluid provides some minimum force to open the valve) while preventing flow in the reverse direction. The ideal diode permits uninhibited current flow in one direction (provided some minimum positive voltage is applied to force the diode into conduction) while limiting reverse current flow to a very small leakage current (provided the negative voltage isn’t as great as to cause the diode to enter breakdown).

These “electrical valves” find utility in numerous applications: rectification, which enhances the average value of a signal and can be used in power supplies; voltage references, in which a desired voltage is achieved as some multiple of the diode *breakdown* voltage; voltage regulators, in which an output voltage is maintained to within some specified tolerance of a desired DC value (useful for power supplies); and tuning circuitry, in which the voltage-variable parasitic capacitance of the diode can resonate with an inductance or active circuit to create a tunable resonant circuit.

**4.2 Theory**

**4.2.1 p-n Junction Basics**

Diodes are formed by the interconnection of p-type and n-type material, so to fully appreciate diode behavior; it is essential to understand the basic physics of such p-n junctions. Recall that a p-type material is a crystal in which there is an excess of holes. Similarly, an n-type material has an abundance of electrons. When two such materials are brought into contact, a charge imbalance results at the junction; and in an effort to achieve charge equilibrium, holes from the p type material diffuse into the n-type material, and electrons from the n-type material diffuse to the p type material. While this movement tends to bring the system toward equilibrium by attempting to *completely* balance the charge differential, it is self-limiting in that the resultant minority charge separation (i.e., positive charge on the n-side, negative charge on the p-side) results in an electric field that opposes diffusion. The resultant equilibrium charge profile is schematically represented in **Figure 4-1**, where the region of charge about the junction is called the *depletion region*.



**Figure 4-1:** Equilibrium charge profile for p-n junction.

Note that a consequence of charge equilibrium is that the *net* charge about the junction is zero. If it weren’t, the electric field lines emanating from the positive charge on the n-side would not have corresponding negative charge on the p-side on which to terminate. The implication is that if, say, the p-type material is doped more heavily than the n-side, so in order to accommodate an equal amount of charge the depletion region is longer on the n-side than the p-side. So, the rule of thumb is that the bulk of the depletion region lies on the more lightly-doped side of the junction. Expressions for the depletion layer width and the fraction lying on each side of the metallurgical junction follow:

 (4.1)

 (4.2)

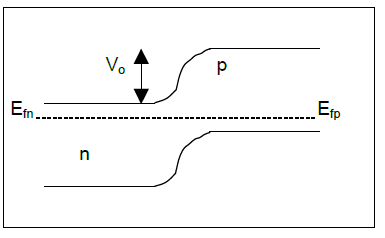
 (4.3)

Note that the electric field at the junction has associated with it a voltage, Vo, called the contact potential or built-in potential. Since voltage is simply defined as the integration of the electric field over distance,

 (4.4)

Since there is no current flow in this state (it is in equilibrium), this voltage does not result in any power consumption. For current to flow, one must apply *additional* voltage external to the p-n junction. This additional voltage creates a disparity in the equilibrium energy profile, and this extra energy finds release as current through the junction.

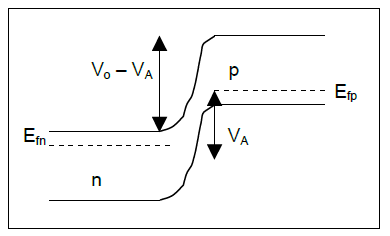
There are three different energy band states that result from an external applied bias. So far, the equilibrium state has been presented and this corresponds to the situation where there is no external bias applied to the device, i.e., VA= 0. This energy band can be seen in **Figure 4-2**. It was explained earlier that a charge imbalance results at the junction when a p-type and n-type material come into contact. The potential difference, Vo, that is a result of this charge imbalance, can be viewed as a potential barrier that needs to be overcome in order for carriers (current) to flow to the external pins of the device. Using the earlier analogy of the valve, an equilibrium state corresponds to the valve being turned off.



**Figure 4-2:** Equilibrium energy band profile for p-n junction

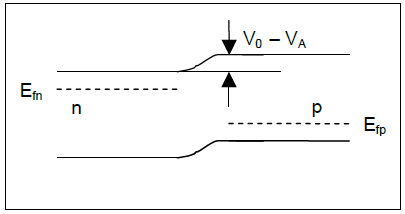
When we apply a *reverse* bias, (VA < 0, where VA is the voltage from the external p-side to the external n-side) the energy band looks like the one in **Figure 4-3**.To accommodate this external voltage in equation 4.1a, one simply replaces Vo by Vo – VA. *Notice:* *you are now subtracting a negative number*, so the bands in the diagram become more separated and the depletion region grows wider. Thus, reverse-bias increases the height of the potential barrier, making it harder for current to flow. However, a very small *drift* current component starts flowing at the onset of reverse bias. This small current is known as the *reverse saturation current* and is very small, usually of the order of 10-15 Amperes.

Going back to the analogy of the valve, a reverse bias still restricts the positive flow of water, but has now allowed the very small flow of water in the opposite direction. The reverse saturation current may be approximated as a constant current, (assuming constant temperature among other things) as the reverse bias is increased up until a certain point where the diode experiences *breakdown*.



**Figure 4-3:** Energy profile for large reverse bias.

When diodes are operated under the *forward bias* condition, a positive external voltage is applied from the external p-side to the external n-side, (VA > 0), which lowers the energy barrier across the junction. Since the barrier is lower, current is able to flow freely and experiences an exponential characteristic as see in equation 4.5. The band diagram looks like the equilibrium diagram and is show in **Figure 4-4**. Notice now that VA is a positive number, so Vo-VA lowers the potential barrier.



**Figure 4-4:** Energy profile of forward bias.

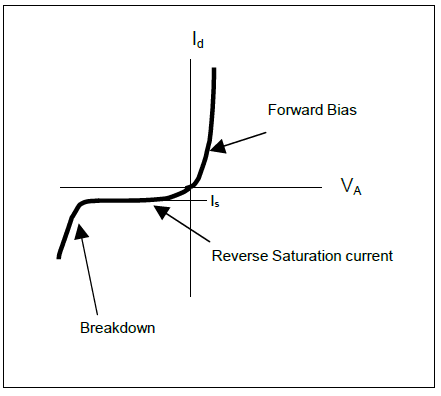
Once again revisiting the valve analogy, this corresponds to opening the valve. How much water flows, or how much current in the diode, is directly dependent on the external applied voltage, VA. Under this condition, the current flowing through the p-n junction is given by

 (4.5)

Where **Is** is the reverse saturation current, **n** is called the ideality factor (typically n has a value between one and two), and **VT** ≈ 25.9 mV at room temperature (27 C or 300 K). This equation validates the valve analogy in that the exponential dependence on the applied voltage indicates that even slight variations in voltage lead to large variations in current. The “force” necessary to open the valve corresponds to a voltage relatively large compared to VT, which is only a modest 26 mV at 300 K (room temperature). *Furthermore, as there isn’t much variation in the diode* *voltage for a useful range of currents, one often talks about a single “turn-on” voltage, which is usually somewhere in the 650mV-to-750mV range for silicon diodes.*

It is often desirable to operate diodes in their *reverse* bias (VA < 0). Such operation is often employed in voltage references. Referring to equation 4.5, the current for negative values of VA approaches –Is. Since Is is often on the order of femto-amperes or even less, it may appear that this reverse bias is useless! However, this equation doesn’t account for a phenomenon called *breakdown*.

Breakdown occurs when some critical reverse bias is applied, at which point the reverse current goes negative extremely rapidly for further reverse bias. There are two kinds of breakdown, namely Zener and avalanche. Zener breakdown is most useful in making voltage references. What happens can be explained from an energy profile perspective in which a reverse bias is applied to the junction. As pointed out earlier, while the depletion width *increases* with reverse bias, the conduction band on the n-side eventually lowers itself to the same *or lower* energy level than the valence band on the p-side. The horizontal separation between these two energy levels diminishes with reverse bias, and there comes a point when this distance is small enough that electrons can easily tunnel through the barrier. When this is the case, Zener breakdown occurs and electron flow is uninhibited – hence the rapid change in current for a “magic” value of reverse bias. By adjusting the doping on the lightly doped side appropriately, one may alter the depletion width W (**Figure 4-1**) according to (4.1), and hence the reverse bias necessary to achieve a small enough distance for tunneling. Zener diodes are diodes for which the doping has been carefully controlled to achieve a desired reverse breakdown voltage. Since the value of breakdown voltage is predictable, Zener diodes make handy reference voltages in discrete design



**Figure 4-5:** I-V characteristics of a diode.

The I-V characteristics of a typical diode are shown in **Figure 4-5**. One may observe that the typical I-V behavior follows what is predicted by equation 4.5. For positive bias, the diode current has an exponential dependence on the applied voltage bias. For a negative bias one can see that the diode hits its “reverse saturation current”, Is. Equation 4.5 fails to account for breakdown, which can be seen in **Figure 4-5**.

**4.2.2 AC signal behavior**

Up to this point, we have implicitly assumed *static*, or DC, diode behavior, that is, the current corresponding to a particular bias voltage is simply one value given by (4.6). In reality it takes some small time for the diode current to increase from zero to its steady-state value after a bias voltage is applied. So, while the familiar relation:

 (4.6)

is true for static problems, a more accurate picture of the situation is obtained by allowing for a term that accounts for *changes* in charge. Thus, for a diode (or for that matter, any real-world phenomenon in which the time-scale of interest is such that the assumption of instantaneous change gives too coarse a view of things), a more accurate equation is the following:

 (4.7)

The first term gives the steady-state, or DC, diode current associated with the recombination charge Q and the lifetime τ before recombination, whereas the second term accounts for the finite exponential rise or fall times associated with abrupt changes in a first-order linear system. Physically, such a delay in moving charge corresponds to capacitance, or in this case a junction capacitance.

**4.2.3 Junction and Diffusion Capacitance**

There are actually two important capacitances associated with diodes: the junction capacitance just noted which accounts for alterations in the junction charge over time, and a diffusion capacitance associated with the delay between a rapid change in current and the attendant delay in junction voltage. Getting an expression for junction capacitance expression is straightforward. The junction capacitance decreases with reverse bias, which is to be expected, since the depletion width increases (to remember this, think of a parallel plate capacitor, for which capacitance diminishes linearly with plate distance). See equation 4.8.

 (4.8)

Where, Ks is the dielectric constant of the semiconductor (for Silicon, Ks=11.8), εo is 8.854 ×10-14 (Farad/cm), A is the area of the depletion layer, and W is the width of the depletion layer. Remember, W increases with increasing reverse bias.

What about the diffusion capacitance? For this, one returns to C=|dQ/dV|, but in this case, one uses a different expression for charge. Also, this capacitance is only important for forward bias, since the charge of interest is directly proportional to current, which is insignificant for reverse bias. The charge is given by

****  (4.9)

 (4.10)

As can be seen, the diffusion capacitance depends linearly with the current through the diode. Thus the diffusion capacitance can change much more abruptly than the junction capacitance.

**4.3 Applications in circuits**

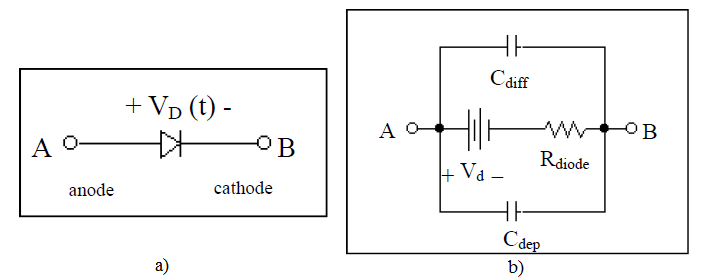
**4.3.1 Large Signal Diode Model**

Until now, this lab has only dealt with a diode when a dc (or biasing) voltage is applied. It is really easy to understand the operation of the diode under any applied bias if one refers to the “valve” analogy used earlier, but what happens when a diode is in your signal path? In analog circuit design we must understand how the diode operates while a signal is superimposed on the dc voltage, or if the dc voltage is varying.

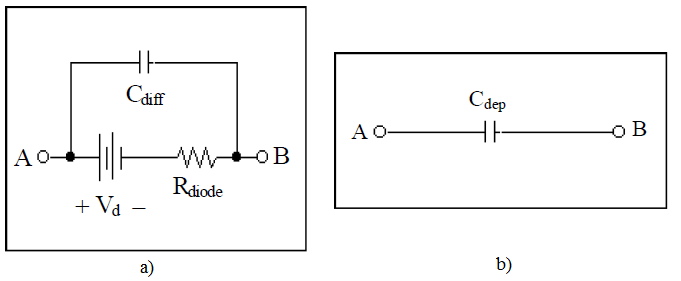
**Figure 4-6** (b) shows a large signal model of the diode in **Figure 4-6** (a). This model includes both the diffusion and depletion capacitance associated with the diode. The complete large signal model in **Figure 4-6** (b) may be simplified to that of the forward-bias model in **Figure 4-7** (a) and to that of the reverse-bias model in **Figure 4-7** (b) depending on the operating bias of the diode (DC bias). When a forward biased voltage is applied to the diode, VD(t) ≥ 0, Cdep becomes negligible compared to the Cdiff. Physically this is attributed to the large current flow and the shrinking of the depletion region.

For the reverse biased case, (VD(t) < 0), the exact opposite occurs. Since little current flows in the opposite direction and the depletion layer gets bigger, Cdep become the dominant capacitance.

As stated before, the depletion capacitance is controlled by the width of the depletion region. This is very useful when a variable capacitor is need for tuning. A reverse biased diode is widely used to tune R, L, C, tank circuits for desired performance.



**Figure 4-6:** (a) Schematic representation of a diode and (b) its complete model, which is a combination of the small and large signal models of a diode.



**Figure 4-7**: (a) Forward bias model and (b) Reverse bias model

Where;

*Vd : diode quiescent voltage* (This is typically around 700mV for Silicon),

*Cdiff : diffusion capacitance*

 (4.11)

Cdep: *depletion capacitance* (mis typically between 1/3 and 1/2 [5]):

 (4.12)

*Rdiode : Forward biased diode diffusion resistance:*

 (4.13)

**4.4 Diode simulation in Spice**

In this section, we investigate the simulation of the I-V characteristics of 1N753.

The syntax for a diode element in Spice is:

dxxx nplus nminus diode\_model\_name.

Where nplus is the positive (anode) node and nminus is the cathode (negative) node of the diode dxxx. Diode\_model\_name is the model name of the diode as specified in the Spice diode model deck.

The simulation of semiconductor devices requires the specification of an appropriate device model deck in Spice. The model deck specifies a particular mathematical model of the device being simulated and the values of the parameters associated with the model. Model parameter values that are not specified default to the default values specified in Spice.

An example of a Spice model deck specification for a diode is shown below, where D1N754 is the name of the diode model. Note that the model deck starts with the keyword .MODEL, followed by the particular diode model name D1N754, followed by the keyword D. The “+” character is a continuation character that indicates that the model deck specification continues on that line.

.model D1N754 D(

+Is=1.616e-15 Rs=1.818 Ikf=0

+N=1 Xti=3 Eg=1.11

+Cjo=120p M=.5117 Vj=.75

+Fc=.5 Isr=1.698e-9 Nr=2

+Bv=6.8 Ibv=2.8814 Nbv=.28248

+Ibvl=1.9426e-6 Nbvl=.27168 Tbv1=485.29u)

\* Motorola pid=1N754 case=DO-35

\* Vz = 7.5 @ 20mA, Zz = 12.5 @ 1mA, Zz = 5.3 @ 5mA, Zz = 2.3 @ 20mA

🖝**Very Important Point:**

*It is very important to start the model deck with the .MODEL keyword, followed by the diode model name and then the keyword D. It is good practice to put the device models at the end of the netlist before the final .END statement.*

**Figure 4-8** is an example of a netlist that can be used to plot the I-V characteristics of the diode

1N754, specified by the model deck named D1N754 in **Figure 4-8**. The voltage across the diode is swept from –7V through 2V in steps of 1mV at circuit temperatures of 27 and 127 ºC. The HSpice simulation results are shown in **Figure 4-9**.

Diode I-V characteristic

\*Written Feb 15, 2005 for EE348L by Bindu Madhavan.

\*Edited Feb 13, 2013 for EE348L by Aaron Curry.

\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

\*\*\*\* options section

\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

.opt post

\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

\*\*\*\* circuit description

\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

d1 2 0 D1N754

r1 1 2 1m

\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

\*\*\*\* sources section

\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

v1 1 0 dc 0

\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

\*\*\*\* specify nominal temperature of circuit in degrees C

\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

.TEMP= 27

\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

\*\*\*\* analysis section

\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

.dc v1 -7 2 1m sweep TEMP poi 2 27 127

\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

\*\*\*\* model deck section

\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

.model D1N754 D(

+Is=1.616e-15 Rs=1.818 Ikf=0

+N=1 Xti=3 Eg=1.11

+Cjo=120p M=.5117 Vj=.75

+Fc=.5 Isr=1.698e-9 Nr=2

+Bv=6.8 Ibv=2.8814 Nbv=.28248

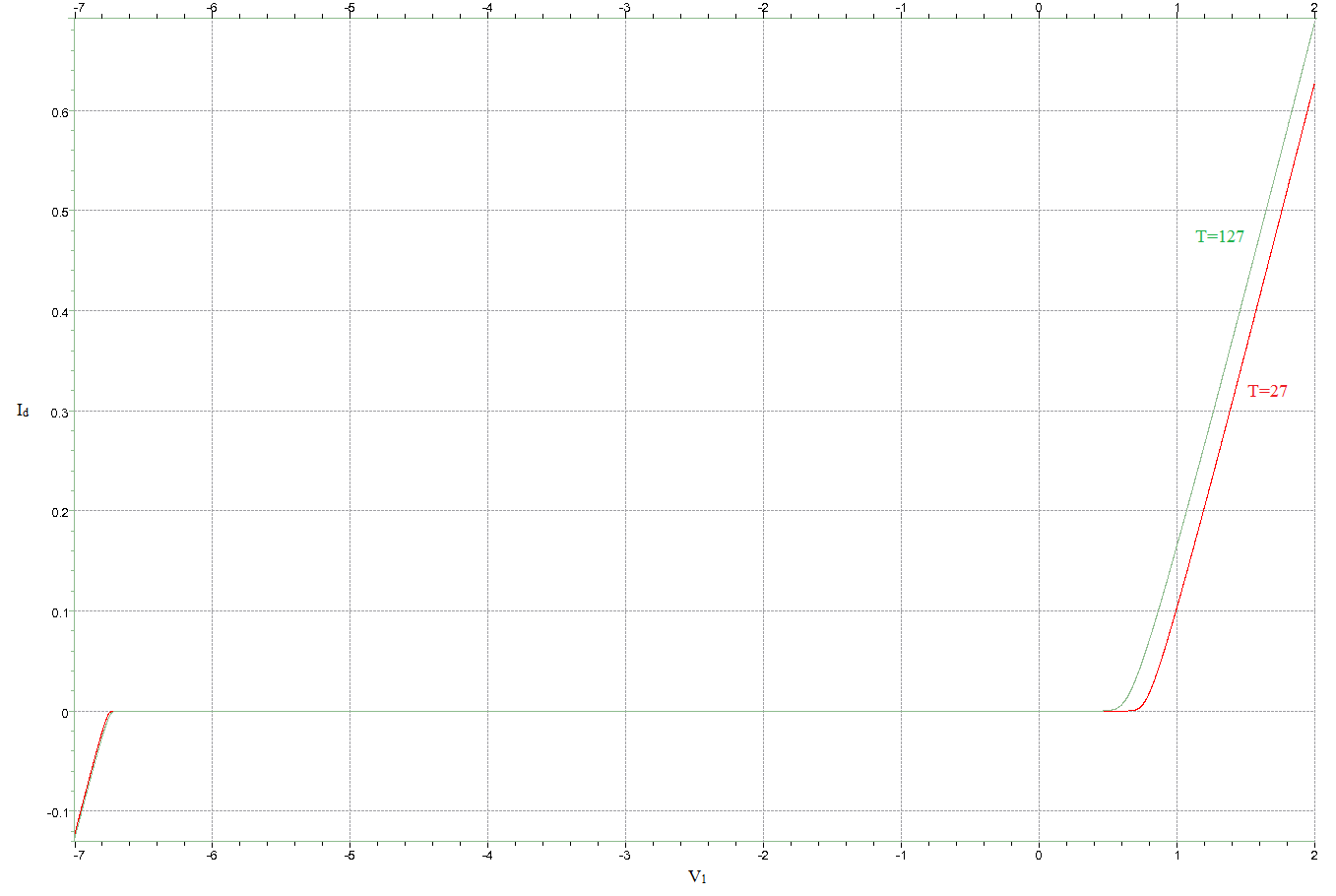
+Ibvl=1.9426e-6 Nbvl=.27168 Tbv1=485.29u)

\* Motorola pid=1N754 case=DO-35

\* Vz = 7.5 @ 20mA, Zz = 12.5 @ 1mA, Zz = 5.3 @ 5mA, Zz = 2.3 @ 20mA

.END

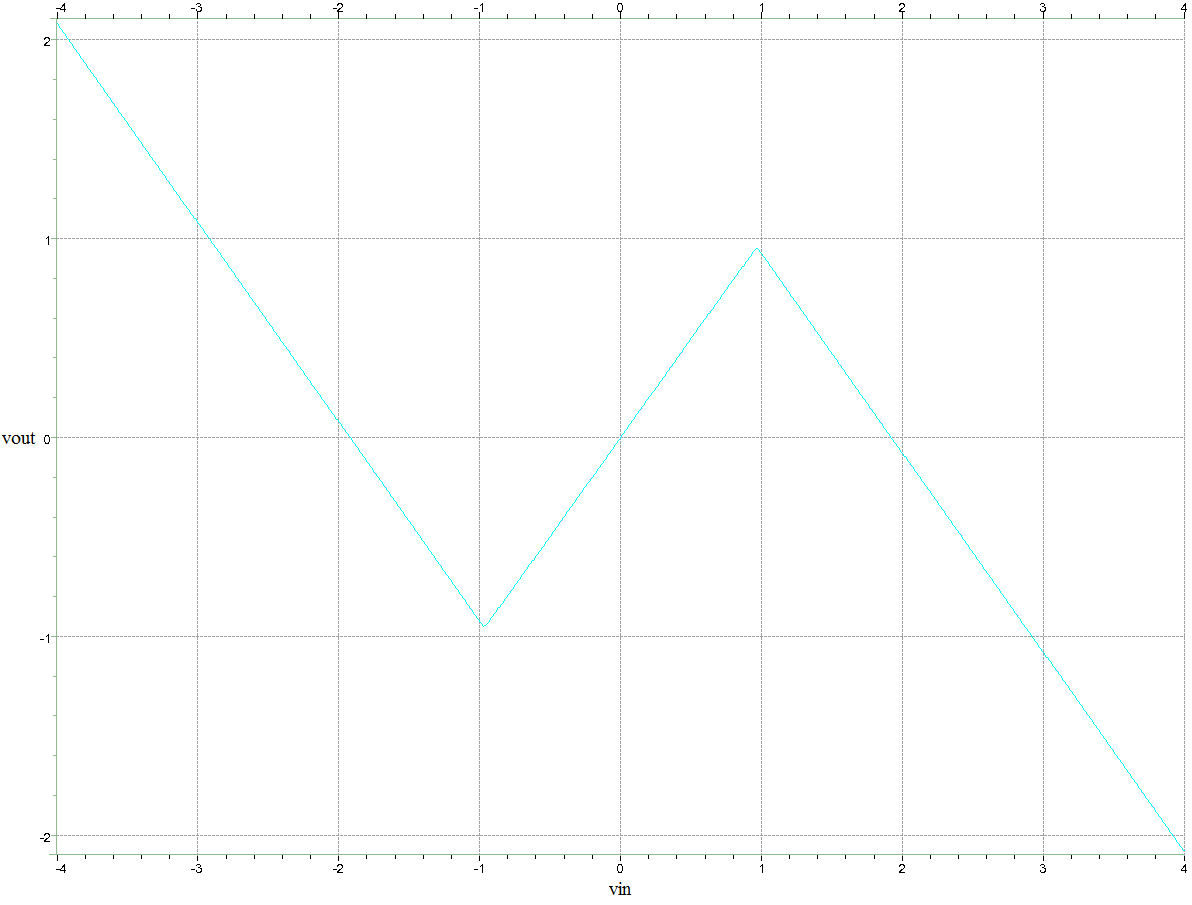
**Figure 4-8:** Spice netlist for obtaining I-V characteristic of diode



**Figure 4-9:** I-V characteristics of diode d1 in **Figure 4-8** for temperatures of 27 ºC and 127 ºC.

**4.5 Transfer characteristic modeling using ideal diodes**

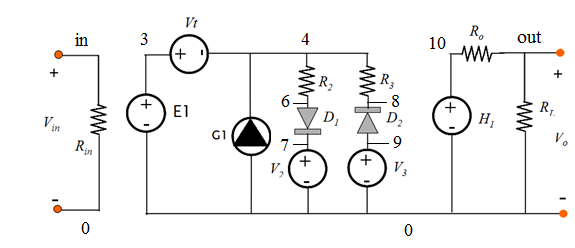
In this section, we look at an example of the use of ideal diodes to model an arbitrary piecewise linear transfer characteristic shown in **Figure 4-10**.



**Figure 4-10:** Piecewise linear voltage transfer characteristic with break points at (-1 V, -1 V), and

(1 V, 1 V)

The circuit that realizes the piecewise linear transfer characteristic shown in **Figure 4-10** is shown in **Figure 4-11**, where D1 and D2 are ideal diodes (approximately modeled in Spice by setting the value of the diode model deck parameter n (**n** in equation (4.5)) to be 0.05, much less than the value of 1 to 2 for realistic diodes. The voltage controlled voltage current source (VCVS) E1 serves the function of a voltage buffer amplifier. The current controlled voltage source (CCVS) H1, which is controlled by the current flowing through the 0V dc-source Vt, serves as a current to voltage buffer. The Spice netlist for realizing the transfer characteristic is shown in **Figure 4-12**, where the plot of Vo versus Vin realizes **Figure 4-10**.



**Figure 4-11:** Circuit realization of piecewise linear voltage transfer characteristic with break points at (-1 V, -1 V), and (1 V, 1 V). Vt is a 0V voltage source, whose current controls the CCVS H1.

PWL behavioral model using ideal diode element (N=0.05)

\*Written Feb 5, 2005 for EE348L by Bindu Madhavan.

\*Edited Feb 13, 2013 for EE348L by Aaron Curry.

\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

\*\*\*\* options section

\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

.opt post

\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

\*\*\*\* subcircuit section

\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

\*\*\*\* circuit description

\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

rin in 0 1e6

e1 3 0 in 0 1

vt 3 4 dc 0

g1 0 4 3 0 3

r2 4 6 0.5

r3 4 8 0.5

d1 6 7 dideal

d2 9 8 dideal

v2 7 0 dc -1

v3 9 0 dc 1

h1 10 0 vt 1

ro 10 out 10

rl out 0 1e5

\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

\*\*\*\* parameters section

\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

\*\*\*\* sources section

\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

v1 in 0 dc 0

\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

\*\*\*\* specify nominal temperature of circuit in degrees C

\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

.TEMP= 27

\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

\*\*\*\* analysis section

\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

.dc v1 -4 4 0.01

\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

\*\*\*\* model section

\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

.MODEL dideal D(IS=1e-15 N=0.05)

.END

**Figure 4-12:** Spice netlist for obtaining piecewise linear transfer characteristic shown in **Figure 4-10**.

**4.6 Conclusion**

The p-n junction is one of the most fundamental elements in circuit design. Understanding of the diode is not only essential to accomplish proper analysis of circuits that contain diodes, but also because it is the fundamental building block of the bipolar junction transistor (BJT). We will see in later labs that a BJT is one of two types of transistor that is used in these labs to produce gain.

**4.7 Revision History**

This laboratory experiment is a modified version of the laboratory assignment created by

Jonathan Roderick, Hakan Durmas, and Scott Kilpatrick Burgess.

**4.8 Reference Reading**

1) Ben G. Streetman. *Solid State Electronic Devices*. Prentice-Hall Inc., Englewood Cliffs, New Jersey, 1990.

2) Richard C. Jaeger. *Introduction to Microelectronic Fabrication*. Addison-Wesley

Publishing Company, Reading, Massachusetts, 1993.

3) S. M. Sze. *Physics of Semiconductor Devices*. John Wiley & Sons, Inc., New York, 1981.

4) Donald A. Neamen. *Electronic Circuit Analysis and Design*. Richard D. Irwin, Chicago,

1996.

5) Gerold W. Neudeck. *Volume II The PN Junction*, Addison-Wesley Publishing Company, Reading, Massachusetts, 1989.

6) Bindu Madhavan, EE348L Laboratory Experiment 3, Spring 2005.

**4.9 Pre-lab Exercises**

**Note:**

• For Spice simulations, use the model deck for 1N754 in **Figure 4-8**.

1. Derive the expression for a diode relating the difference in two bias voltages to the corresponding bias currents. Assume the diode is in the forward active region. For a 10:1 range of currents at room temperature, what is the resultant change in bias voltage? What does this tell you about the current-voltage relationship of a diode? Is it very sensitive? Explain your answer. nVT = 25.9 mV small changes in the voltage result in drastic changes in current in forward bias
2. Refer to **Figure 4-15**. Obtain the following plots of the *forward* bias (0-2V) I-V characteristics of the diode 1N754 with HSpice for R1=1k Ω and 10k Ω.

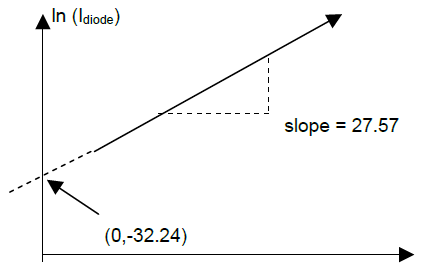
* The difference in diode voltage for R1=1k Ω and 10k Ω.
* The ratio of diode current for R1=1 k Ω and 10k Ω.
* The derivative of the current through the diode versus input voltage for each resistance value.

**Hint:** For the difference in diode voltage and ratio of diode current plots you can drag each plot into the equation builder and take the difference/ratio. For the derivative, you can use the slope function in the equation builder.

1. When r1 is 1kΩ, what does the slope of the diode current saturate at? Explain numerically why the slope is what it is. Near the value of -1/r1 979\*10^-6
2. When r1 is 10kΩ, what does the slope of the diode current saturate at? Explain numerically why the slope is what it is. Near the value of -1/r2 98.6\*10^-6
3. What does the difference in diode voltage saturate at? What does the ratio of diode current saturate at? Does this verify your response in exercise 1?

**Hint:** the slope has to do with the value of R1. -60 mV difference, 0.1 ratio, yes it does.

1. The imperfect manufacture of diodes results in devices that don’t follow exactly the standard relation given in problem number 1. Any resistance at the diode contacts or space-charge recombination causes the I-V relation to be slightly less than exponential (i.e., the resistance linearizes the I-V relationship). This non-ideality is usually accounted for by incorporating a non-ideality factor “n” as seen in equation 4.5. Consider the I-V sketch shown below, where the current is shown on a log axis. What are the saturation current and non-ideality factor for this diode? As simple as this exercise may seem, in practice, a parameter analyzer set to display diode current vs. voltage on a log-linear plot is the method employed to extract the saturation current and non-ideality factor.

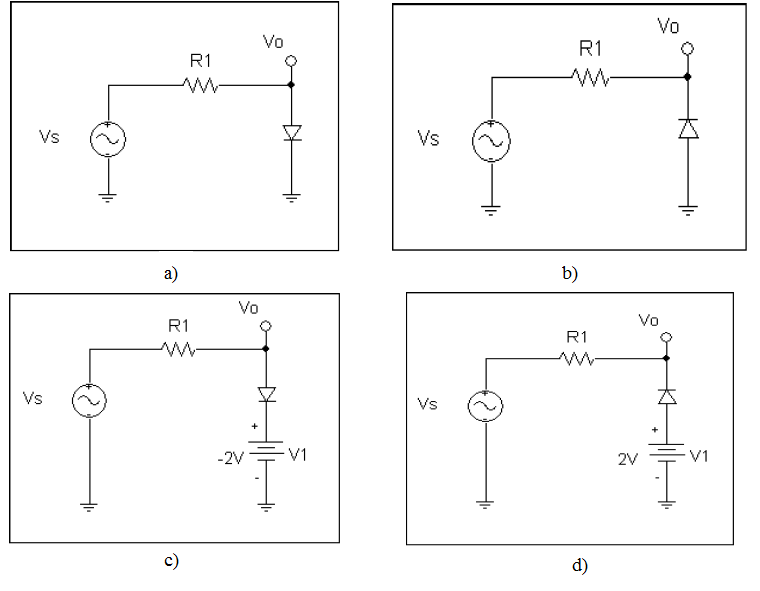


**Figure 4-13:** I-V sketch of a diode.

1. Refer to the circuit in **Figure 4-16**. Remember that a single pole system has a time constant that is approximately equal to the inverse of the –3dB bandwidth (in rad/s). Build the circuit in HSpice and perform ac sweeps to determine the -3dB bandwidth for different bias values. Set Vbias to .3V and .5V. Calculate the capacitance of the diode using the known value for R for each bias. Do the same for Vbias -.3V and -.5V.
2. Does the capacitance of a diode change with respect to the bias voltage?
3. Which capacitance dominates for forward bias? Does the capacitance increase or decrease with increasing forward bias? Does HSpice verify this?
4. Which capacitance dominates for reverse bias? Does the capacitance increase or decrease with increasing reverse bias? Does HSpice verify this?
5. Under which bias condition (forward or reverse) does the capacitance change more drastically?

**Hint:** See section 4.2.2 and 4.2.3.

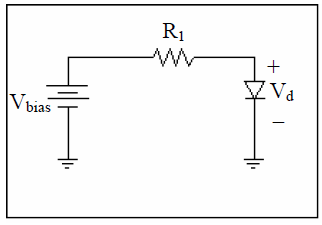
1. Predict and sketch the output waveforms of the circuits in **Figure 4-14** (a), (b), (c), and (d). The signal source should have a frequency of 5kHz and a 3 volt amplitude and R1=1k. For each prediction, give a qualitative explanation or deductive reasoning of why you came up with what you did. If it helps, use the “valve” analogy. Verify your predictions with Spice.

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**Figure 4-14:** (a), (b), (c) and (d) for pre-lab exercise 3. R1 = 1 KΩ. The signal source has a frequency of 5 kHz and amplitude of 3V.

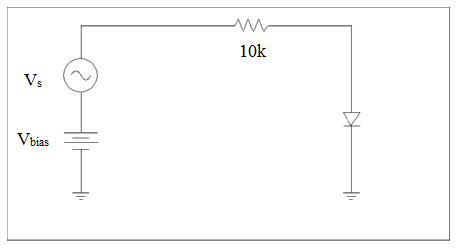
* 1. **Lab Exercises**
* Remember that an amplitude of 50mV corresponds to a Vpp of 100mV.
* Submit plots relevant to reach question in your lab report.

1. Build the following circuit, using a 1 KΩ resistor. Put Vbias to 1V. Measure the current and diode voltage. Replace the resistor with a 10 KΩ resistor. Re-measure the current and diode voltage for the same Vbias (The current should have dropped by approximately one order of magnitude). What is the relative change in current, namely by what multiplicative factor does the current increase or decrease by? What is the change in diode voltage? Do the results agree with your estimate in pre-lab Exercise 1?



**Figure 4-15:** Circuit schematic for Lab exercise 1

1. Use the same circuit as in the previous exercise, replacing the resistor with a potentiometer (pot). Vary the pot from 1-10 KΩ, and monitor the current and diode voltage for ten different potentiometer values. Use a wider range pot to vary the resistance from 10-100 KΩ, monitoring the current and diode voltage for ten more potentiometer values. Plot both I-V characteristics on the **SAME** log-linear graph, fit a line to the data, and from the slope and intercept, determine the non-ideality factor and saturation current, respectively.
2. Build the circuit in **Figure 4-16**. Remember that a single pole system has a time constant that is approximately equal to the inverse of the –3dB bandwidth (in rad/s). Use the internal DC offset of your signal generator to produce positive bias on the diode and measure the time constant with an oscilloscope while sweeping Vs. Try to make the amplitude on Vs as small as possible. Set Vbias to .2V and .4V. Calculate the capacitance of the diode using the known value for R for each bias. Do the same for for Vbias -.2V and -.4V.
3. Does the capacitance of a diode change with respect to the bias voltage?
4. Does the capacitance increase or decrease with increasing forward bias?
5. Does the capacitance increase or decrease with increasing reverse bias?
6. Under which bias condition (forward or reverse) does the capacitance change more drastically?
7. Do your results verify what you got in pre-lab exercise 4?



**Figure 4-16:** Circuit schematic for Lab exercise 3.

1. Build the circuits (**Figure 4-14** (a), (b), (c), and (d) in exercise #4 of the pre- lab. Using an oscilloscope, capture ore sketch each output and compare them to your predictions. Are they similar? Explain any discrepancies.
2. Find an expression for vout in Figure 4-11. Explain how the circuit in Figure 4-11 generates the piecewise linear characteristic in Figure 4-10.

*Hint: The piecewise linear characteristic is determined by the values of G1, R2, R3, V2, and V3. Determine how the current through Vt is dependent on the branches (G1), (V2, D1, R2), and (V3, D2, R3). Assume that diodes D1 and D2 are ideal diodes. You will need to solve for Vt in three different regions: -4<vin<-1, -1<vin<1, and 1<vin<4.*